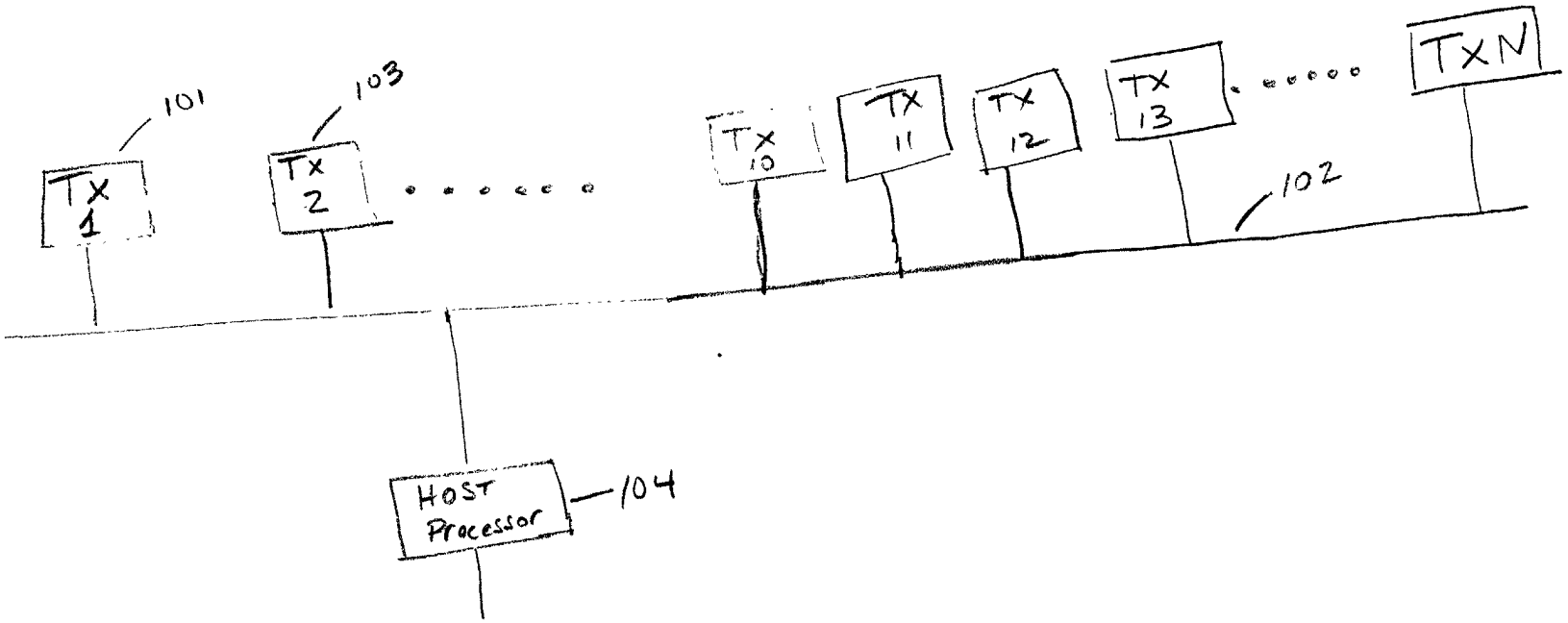

TX 1
101
TX 2
103
TX 10
TX 11
TX 12
TX 13
TXN
102
HOST Processor
104

Fig. 1

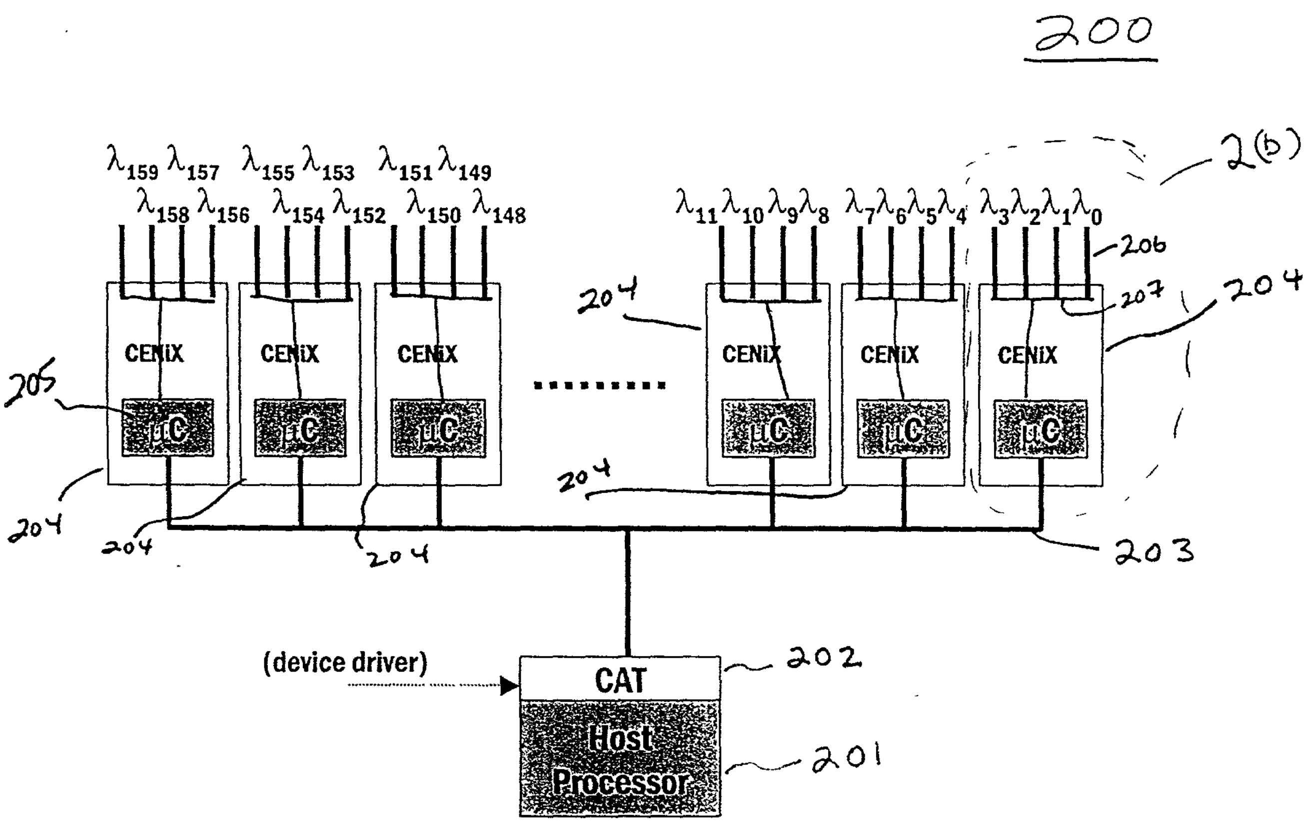

200
2(b)
λ159 λ157
λ158 λ156
λ155 λ153
λ154 λ152
λ151 λ149
λ150 λ148
λ11 λ10 λ9 λ8
λ7 λ6 λ5 λ4
λ3 λ2 λ1 λ0
206
207
204
205
CENiX
μC
203
(device driver)
CAT
202
Host Processor
201

Fig. 2 (a)

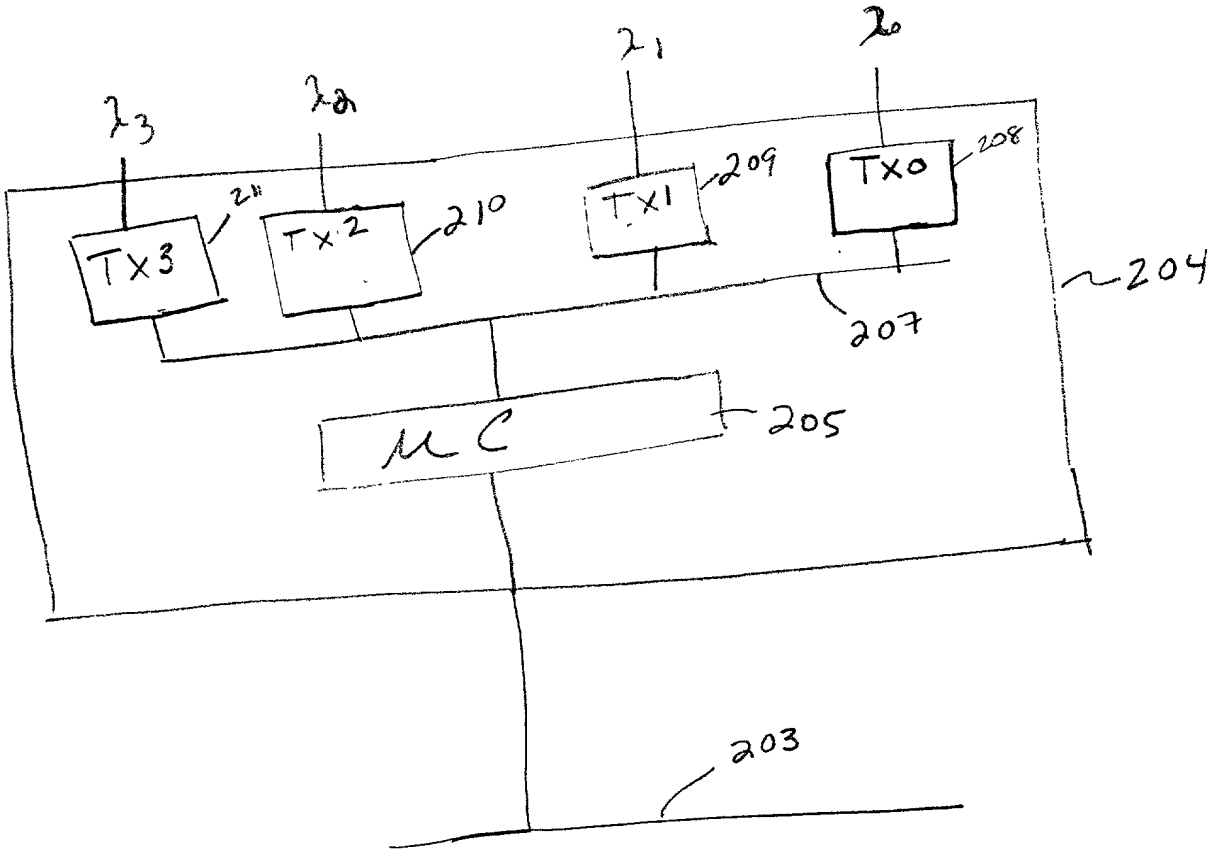


Fig. 2(b)

(Channel Access Table Example) 212

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	0	0x200
2	0	0x400
3	0	0x600
4	4	0x000
5	4	0x200
6	4	0x400
7	4	0x600
⋮	⋮	⋮
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

Fig. 2(c)

Fig. 3

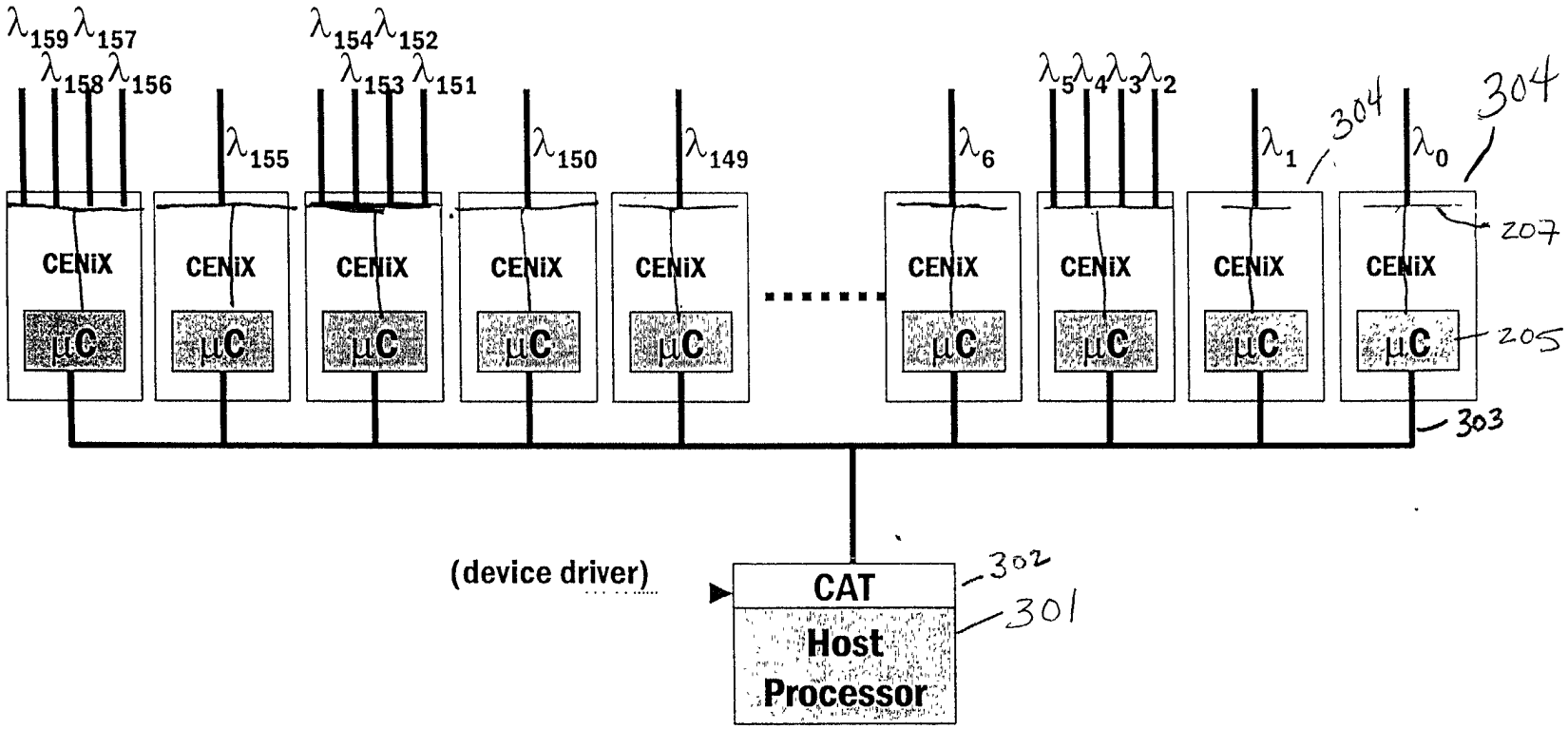

λ159 λ157
λ158 λ156
λ154 λ152
λ153 λ151
λ155
λ150
λ149
λ6
λ5 λ4 λ3 λ2
λ1
λ0
304
304
207
205
303
CENiX
µC
(device driver)
CAT
Host
Processor
302
301

Fig. 4

400

(Channel Access Table Example)

Channel Address	Physical Address	Memory Offset
0	0	0x000
1	1	0x000
2	2	0x000
3	2	0x200
4	2	0x400
5	2	0x600
6	6	0x000
⋮	⋮	⋮
154	151	0x600
155	155	0x000
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

Fig. 5

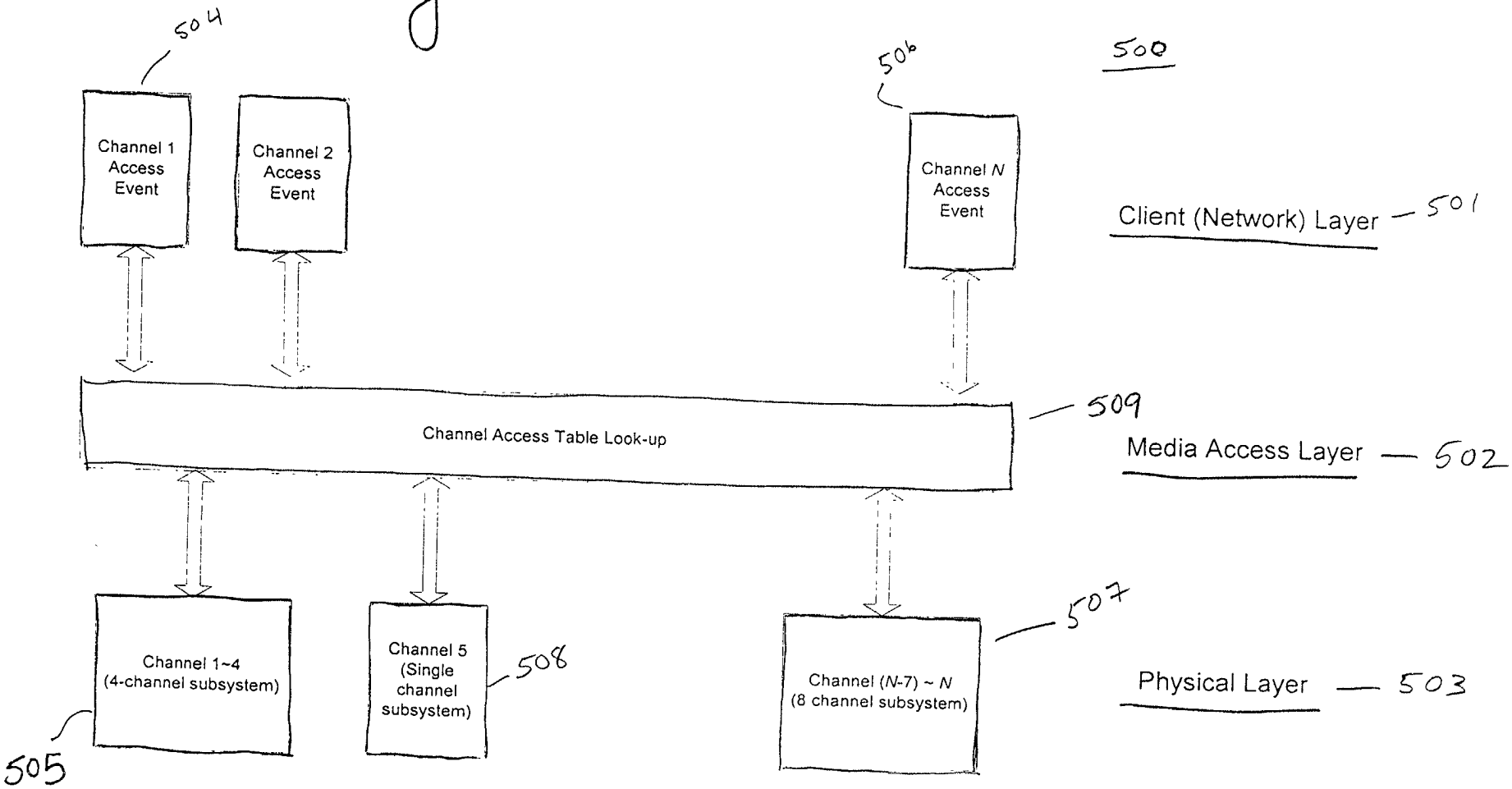
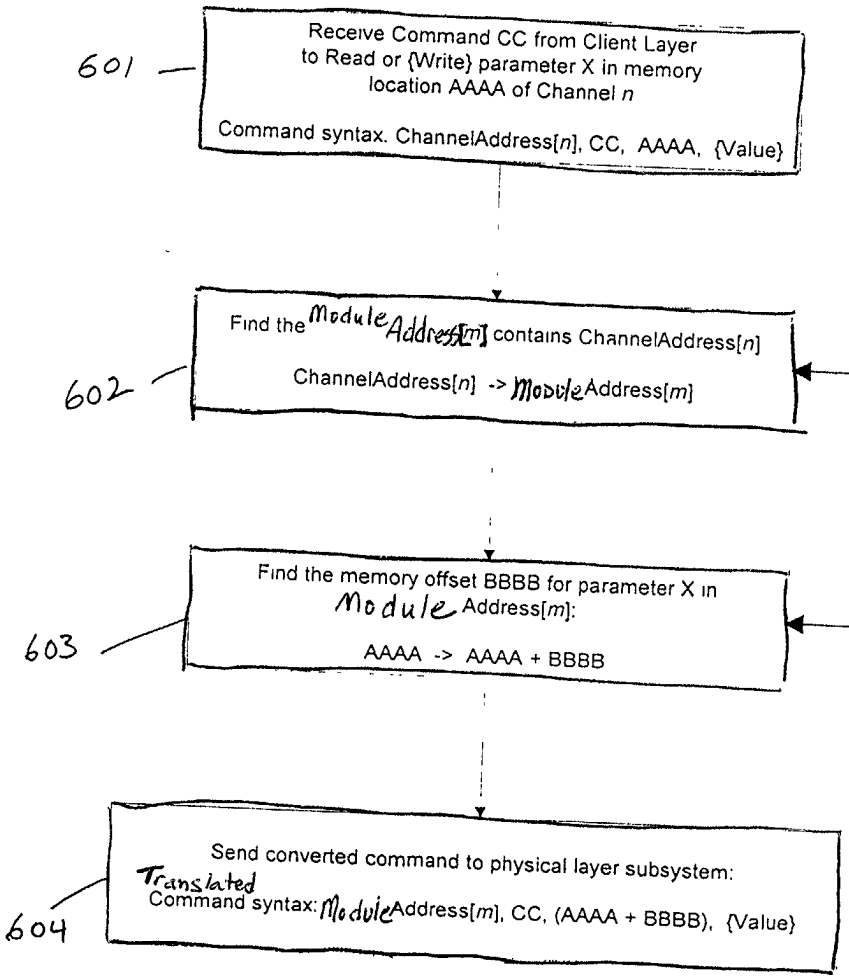

504
506
500
Channel 1 Access Event
Channel 2 Access Event
Channel N Access Event
Client (Network) Layer
501
Channel Access Table Look-up
509
Media Access Layer
502
Channel 1~4 (4-channel subsystem)
505
Channel 5 (Single channel subsystem)
508
Channel (N-7) ~ N (8 channel subsystem)
507
Physical Layer
503

FIG. 6



(Channel Access Table Example)

Channel Address *n*	Module Address *m*	Memory Offset BBBB
0	0	0x000
1	1	0x000
2	2	0x000
3	2	0x200
4	2	0x400
5	2	0x600
6	6	0x000
⋮	⋮	⋮
154	151	0x600
155	155	0x000
156	156	0x000
157	156	0x200
158	156	0x400
159	156	0x600

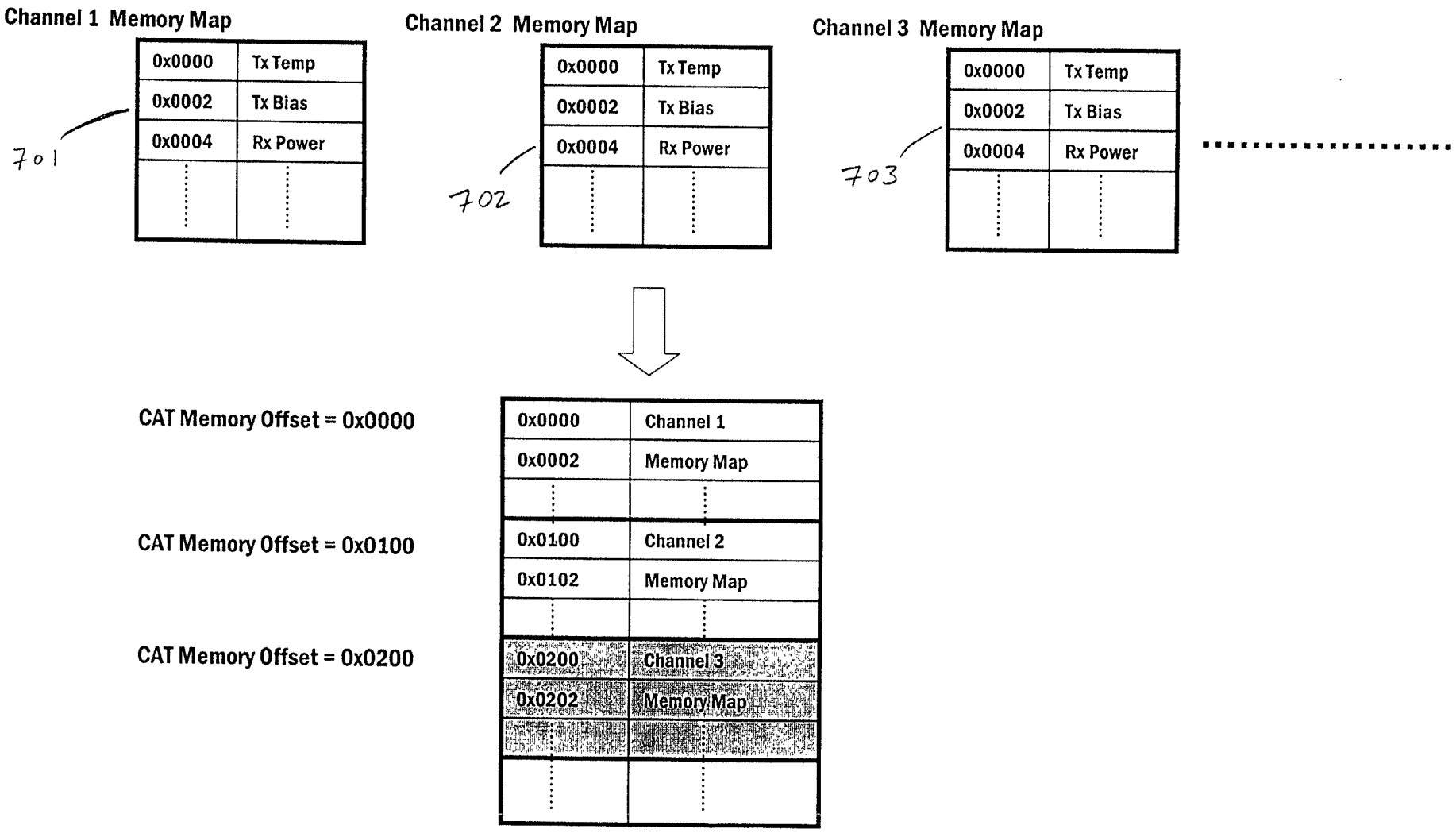

Channel 1 Memory Map
0x0000
Tx Temp
0x0002
Tx Bias
0x0004
Rx Power
701
Channel 2 Memory Map
0x0000
Tx Temp
0x0002
Tx Bias
0x0004
Rx Power
702
Channel 3 Memory Map
0x0000
Tx Temp
0x0002
Tx Bias
0x0004
Rx Power
703
CAT Memory Offset = 0x0000
CAT Memory Offset = 0x0100
CAT Memory Offset = 0x0200
0x0000
Channel 1
0x0002
Memory Map
0x0100
Channel 2
0x0102
Memory Map
0x0200
Channel 3
0x0202
Memory Map

Fig. 7